

USB4 1.0 ENGINEERING CHANGE NOTICE FORM

Title: TBT3 Single Lane 1 Support

Applied to: USB4 Specification Version 1.0

Brief description of the functional changes:
Removes the requirement to have Lane 1 as a separate Single-Lane Link in TBT3-Compatible Routers.

Benefits as a result of the changes:
Reduced complexity for TBT3-Compatible Routers.

An assessment of the impact to the existing revision and systems that currently conform to the USB specification:
None

An analysis of the hardware implications:
None

An analysis of the software implications:
None

An analysis of the compliance testing implications:
Remove the tests for Lane 1 Single-Lane Link.

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Actual Change

(a). Section 13.2.3.1, USB4 Link Transitions, Page 535

To Text:

When TBT3 Mode is established on the Link, a USB4 Port shall support the transitions described in Section 4.2.1.6.5.4 with the following changes:

- For a Device Router that supports TBT3 Mode on its Upstream Facing Port, all USB4 Ports shall support operation with two ~~independent~~ Single-Lane Links. Unlike Section 4.2.2, this configuration is not just a transient state between Link Initialization and Lane Bonding. When operating with two Single Lane Links, a USB4 Port is only required to support traffic on Lane 0. In TBT3 Mode, both Links may operate as independent Single Lane Links and are configured and managed separately by the Connection Manager.



CONNECTION MANAGER NOTE

A Connection Manager shall not set the Lane Bonding bit to 1b if ~~either of the following are true:~~

~~A~~a Path other than Path 0 is enabled across the Lanes being bonded.

- ~~A Lane 1 Adapter is the Upstream Adapter.~~

(b). Section 13.2.4.1, Entry to Sleep, Page 535

To Text:

After the *Enter Sleep* bit is set to 1b in all Ports, a Device Router shall do the following for each USB4 Port:

- Transition the Lane Adapters to CLd state.
- If any of the following conditions apply, the USB4 Port shall go through disconnect:
 - For Lane 0 in a USB4 Port:
 - The *Lane 0 is Inter-Domain* bit is 0b and the *Lane 0 Configured* bit is 0b.
 - The *Lane 0 is Inter-Domain* bit is 1b and the *Inter-Domain Disconnect on Sleep* bit is set to 1b.
 - ~~For Lane 1 in a USB4 Port:~~
 - ~~The *Lane 1 is Inter-Domain* bit is 0b and the *Lane 1 Configured* bit is 0b.~~
 - ~~The *Lane 1 is Inter-Domain* bit is 1b and the *Inter-Domain Disconnect on Sleep* bit is set to 1b.~~

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(c). Section 13.2.4.2, Behavior in Sleep State, Page 536

To Text:

If ~~Lane 0 of a~~the USB4 Port is disconnected while in Sleep state, then the internal *Lane 0* is *Inter-Domain state*, ~~and Lane 0 Configured state~~, *Lane 1 is Inter-Domain state, and Lane1 Configured state* listed in Table 13-9 shall ~~both~~all transition to 0b.

~~If Lane 1 of a USB4 Port is disconnected while in Sleep state, then the internal Lane 1 is Inter-Domain state and Lane1 Configured state listed in Table 13-9 shall both transition to 0b.~~

(d). Section 13.3.3, Connectivity Rules, Page 537

To Text:

~~This section only applies to a Device Router that supports TBT3 Compatibility on its UFP.~~

~~A Device Router shall support the Connectivity rules defined in Section 5.2.5 for both the Lane 0 Adapter and Lane 1 Adapter in a USB4 Port. For example, where Section 5.2.5 requires that "A Router shall be able to forward a Control Packet received on any Lane 0 Adapter to the Control Adapter" this section also requires that a Device Router shall be able to forward a Control Packet received on any Lane 1 Adapter to the Control Adapter.~~

(e). Section 13.5, Time Synchronization, Page 540

To Text:

When a USB4 Port is operating as two Single-Lane Links in TBT3 mode, the Time Sync Handshake shall occur on Lane 0 ~~when the Lane 0 Adapter is in CL0 state. If the Lane 0 Adapter is not in the CL0 state but Lane 1 Adapter is in the CL0 state, the Time Sync Handshake may occur on Lane 1.~~